REMARKS

Claims 1-20 are all the claims pending in the application. Claims 21-26 are cancelled as being directed to a non-elected invention/species. Claims 3, 10, and 17 stand objected to only as being dependent upon a rejected base claim, and are indicated to be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claims. Claims 3, 10, and 17 have been rewritten in independent form to place them in condition for immediate allowance. An excess fee payment accompanies this Amendment to pay for the excessive number of independent claims.

Claims 1-2, 5-9, 11-16, and 18-20 stand rejected on prior art grounds. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-2, 5-9, 11-16, and 18-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hsu et al. (US Patent Publication 2002/0171101 A1). Applicants respectfully traverse these rejections based on the following discussion.

A. The Rejection Based on Hsu et al.

Hsu discloses a memory cell structure, in Figure 2 for example, that includes separate transistors C1, C2 connected to true and complement bitlines. The Office Action argues that only one of the sources of the two different transistors is connected to ground 30. However, Figures 1, 2, and 4-13 of Hsu actually disclose that each pair of transistors shares a common source. Therefore, it is impossible for the structure disclosed in Hsu to have only one of the sources of the two separate transistors connected to ground.

This is contrary to the claimed invention that has "only one of said first source and said second source is connected to ground" (independent claims 1, 8, and 15). As shown in Applicants' Figure 1, a logical 0 is achieved by having the source of the true transistor connected to ground, while the source of the complementary transistor is left

floating. To the contrary, a logical 1 is achieved by having the source of the true transistor electrically insulated (floating), while the source of the complementary transistor is tied to ground. Therefore, the cell 100 represents a logical 0 because the source 117 of the complementary transistor 115 is left floating, while the source 110 of the true transistor 111 is tied to ground 104. To the contrary, cell 101 represents a logical 1 by having the source 123 of the true transistor 120 floating and the source 122 of the complementary transistor 121 connected to ground 107.

In operation, both true and complement bitlines are precharged to VDD. When the wordline voltage rises, the transistors connected to ground will conduct and pull its respective bitline towards ground. The transistor that has its source floating will have no affect on its respective bitline which should maintain a voltage near VDD. If the true transistor pulls the true bitline towards ground while the complement bitline remains near VDD, a logical 0 is read. If the complement transistor pulls the complement bitline towards ground while the true bitline remains near VDD, a logical 1 is read. Note also that, since drains are always connected to the bitlines, all bitlines will have approximately the same capacitance.

This is fundamentally different than the structure disclosed in Hsu which utilizes a common source for each of the pairs of transistors. By utilizing a common source, both transistors will always have the source connected to the same voltage level. Thus, one transistor cannot be connected to ground while the other transistor is insulated, in the structure disclosed in Hsu.

In view the forgoing, Applicants respectfully submit that independent claims 1, 8, and 15 are patentable over Hsu because Hsu does not teach or suggest that "only one of said first source and said second source is connected to ground." Further, not only are independent claims 1, 8, and 15 patentable, but also, dependent claims 2, 4-7, 9, 11-14, 16, and 18-20 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also of because of the additional features of the invention they define. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

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II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-20, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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